

Infiltration behaviour of an internal electrode and electrical properties of multilayer capacitors by electrode infiltration

TAE-SUNG OH, CHANG-BONG LEE, YOON-HO KIM

Fine Ceramics Laboratory, Korea Institute of Science and Technology, PO Box 131, Cheongryang, Seoul, Korea

The infiltration behaviour of a tin melt, as an internal electrode, to the porous layers, and the electrical properties of multilayer ceramic capacitors was investigated by electrode infiltration. By preventing green-state delamination between the dielectric green sheet and the carbon paste, uniform porous layers, 5 μm thick, could be formed after sintering. When 15 vol% ceramic pillars were added to the carbon paste, the porous layer of the sintered samples could be considered as a porous solid formed by many pores larger than 4 μm . The critical pressure for the infiltration of tin melt into such a porous layer was found to be 0.5 MPa. With a high infiltration pressure, the resistivity of multilayer capacitors was decreased to 10^8 – $10^9 \Omega \text{cm}$ due to the growth of micro-defects formed on the surface of the dielectric layers during the lamination process.

1. Introduction

In recent years, there has been a great demand in the electronics industry for multilayer ceramic chip capacitors, which are one of the main components indispensably required to build up electronic circuits. Multilayer ceramic capacitors have large capacitance per unit volume and can be soldered directly on the printed circuit boards by surface mounting technology to meet the trend of miniaturization and high functionality of modern electronic devices [1, 2]. To reduce the processing cost of multilayer capacitors, dielectric formulations and process technology have been extensively investigated to assess use of cheap metals as internal electrodes: dielectric formulations for base-metal electrodes such as nickel and iron [3–5] and the process for internal electrode infiltration [6–11].

In the case of multilayer capacitors with nickel or Ag/Pd electrodes, dielectric formulations and sintering conditions are limited by electrode materials [3–5, 11, 12]. Furthermore, delamination has been observed to be due to the thermal expansion mismatch between ceramics and metals because metal-electrode paste is screen-printed on dielectric green sheets and co-fired [13]. In contrast, delamination by thermal expansion mismatch can be eliminated in the electrode-infiltration method [14, 15] because the dielectric layers are sintered and then the electrode is infiltrated into porous layers formed by complete burn-out of carbon paste at temperatures below 500 °C during sintering. In addition, dielectric formulations with optimum electrical and mechanical properties can be selected and sintered in air with an optimum temperature–time schedule. With such advantages, as

well as cost reduction with a base metal electrode such as tin and lead, many patents [6–11, 16–20] have been filed for the fabrication of multilayer ceramic capacitors by electrode infiltration, after Rutt [8]. However, most investigations have focused on the process itself and little has been reported on the effects of infiltration parameters on the electrical properties of multilayer capacitors.

In this study, the formation of porous layers and the effects of process parameters, such as infiltration pressure and time, on the electrical properties of multilayer capacitors by electrode-infiltration have been studied by observing the microstructure before and after electrode infiltration, and by measuring the dielectric constant, dissipation factor and insulation resistance of multilayer capacitors.

2. Experimental procedure

Low-temperature firing X7R powder, average particle size of 1.2 μm , where small amounts of Nb_2O_5 , Co_3O_4 , ZnO and MnCO_3 were added to BaTiO_3 [1, 21], was used as a dielectric material for multilayer capacitors in this study. After mixing X7R powder with acrylic binder using alumina balls in a plastic jar for 24 h, a dielectric green sheet of 60 μm thickness was obtained by the doctor-blade method. Using an organic vehicle composed of 80 ml turpentine oil, 14 g acrylic resin, 1.5 g lecithin and 1.5 g ethyl cellulose [7], carbon paste was made to form porous layers during sintering by vibro-milling of 5 g C and 5 g calcined X7R powder with 20 g organic vehicle for 30 min. Carbon pastes containing 2.5 and 10 g calcined X7R powder were also made to investigate the effects of

pillar content in the porous layers on the electrical properties of multilayer capacitors. After carbon paste was screen printed on dielectric green sheets and dried in air for 24 h, six layers of green tapes were laminated at a pressure of 80 kg cm^{-2} for 5 min after heating for 30 min at 130°C and then cut to obtain green chip samples. Chip specimens ($10 \text{ mm} \times 11 \text{ mm}$) with 10 mm long porous layers (Fig. 1) were made by sintering green chips at 1140°C for 2 h after complete burn-out of carbon and the organic vehicle in the carbon paste by holding for 10 h at 500°C . The thickness of the dielectric layer shrank from $60 \mu\text{m}$ to about $50 \mu\text{m}$ after sintering.

Sintered chips were charged into an autoclave, as shown in Fig. 2, which was then evacuated to 1 Pa vacuum during heating the autoclave to 260°C . Tin was then infiltrated into the porous layers of chip specimens by dipping samples into a tin melt bath and applying an external pressure ranging from 0.2–1.5 MPa using nitrogen gas. After holding the samples in the tin melt bath for 0.5–180 min, the samples were withdrawn from the melt bath and the autoclave was cooled to a temperature below the melting point of tin without removing the nitrogen gas pressure. After samples were removed from the auto-

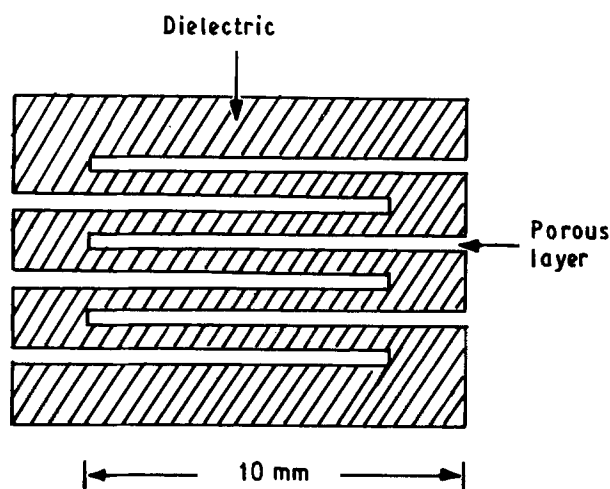


Figure 1 Schematic illustration showing cross-section of a sintered chip specimen with 10 mm long porous layers.

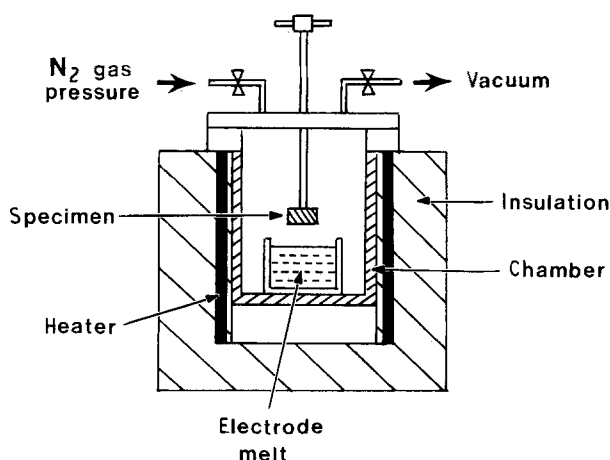


Figure 2 Schematic illustration of an experimental apparatus for electrode infiltration into porous layers.

clave, external electrodes were formed by applying room-temperature silver paste to the ends of the tin-infiltrated samples.

The capacitance and dissipation factor of tin-infiltrated capacitors were characterized using an LCR Meter at 1 kHz and the insulation resistance was measured by a high-resistance meter at 100 V d.c. Capacitance is dependent on the number and thickness of the dielectric layers and the electrode area. Therefore, in this study, dielectric constants calculated from the measured capacitance values were used to characterize quantitatively the infiltration behaviour. Tin infiltration into porous layers, and delamination between dielectric and porous layers, were characterized by observing the microstructures of fracture and polished surfaces of chip specimens using scanning electron microscopy (SEM).

3. Results and discussion

3.1. Formation of uniform porous layers

For the fabrication of multilayer ceramic capacitors by electrode infiltration, carbon paste of optimum properties is required to form uniform porous layers. Carbon paste should be completely burnt-out without any residue, and have sufficient adhesion to the dielectric layers stacked above, after the lamination process, to minimize the delamination before sintering [13].

Fig. 3 shows the microstructure of sintered chip specimens before electrode infiltration. For the sample of Fig. 3a, where carbon paste was made using an organic vehicle composed of 80 ml turpentine oil, 14 g acrylic resin, 1.5 g lecithin and 1.5 g ethyl cellulose [7], uniform porous layers were not formed due to the green-state delamination before sintering. Such green-state delamination was exaggerated during cutting of the laminated dielectric body into green chip specimens [13]. On increasing the adhesion of the carbon paste to the dielectric green sheet by changing the amount of each constituent of the organic vehicle, however, $5 \mu\text{m}$ thick uniform porous layers could be obtained, as shown in Fig. 3b.

3.2. Effects of infiltration parameters

Fig. 4 shows the dielectric constant, as a function of temperature, of a multilayer capacitor infiltrated with tin for 1 min at an external pressure of 1.5 MPa and a disc sample formed by sintering after laminating only ceramic green tapes without carbon-paste interlayers. Dielectric constants of 2670 and 2180 were obtained at 40°C for the disc-type and multilayer samples, respectively. The dissipation factor was below 2% for both disc-type and multilayer capacitors.

In general, the capacitance of electrode-infiltrated samples is decreased by the reduction of electrode area with high volume percentage of pillars or by collapse of porous layers during sintering with low volume percentage of pillars. Thus, the optimum pillar content in the carbon paste has been reported to be about 10 vol% [22, 23]. Fig. 5 illustrates the variation of the dielectric constant of multilayer samples as a function of the pillar content in the carbon paste. The volume

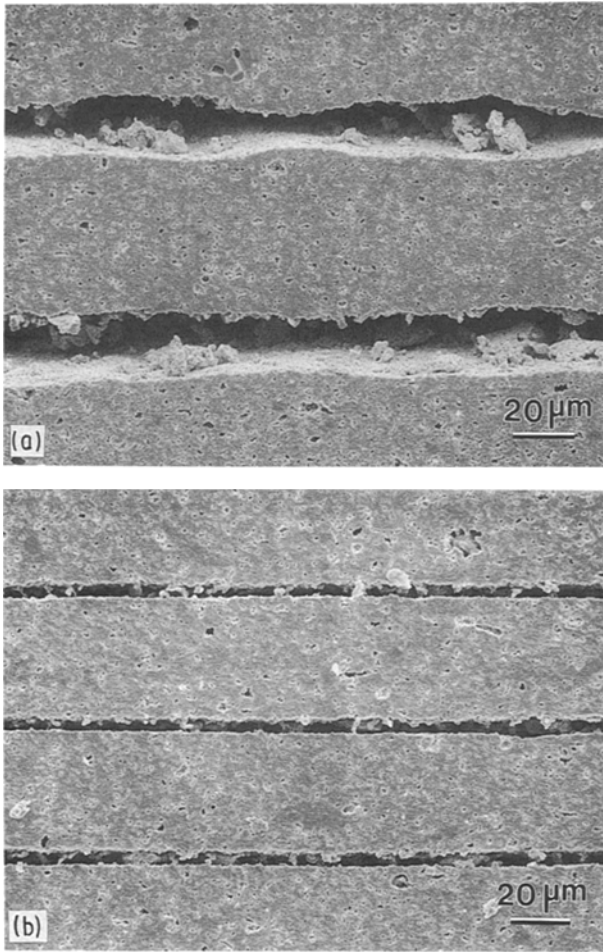


Figure 3 Scanning electron micrographs of sintered chips before electrode infiltration showing porous layers (a) with and (b) without green-state delamination.

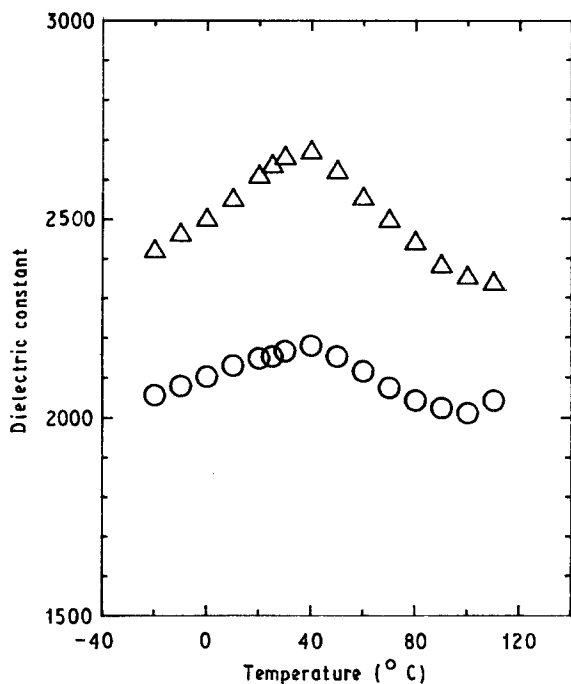


Figure 4 Dielectric constant, as a function of temperature, of (Δ) a disc-type capacitor and (○) a multilayer capacitor. For the multilayer sample, tin was infiltrated for 1 min at 1.5 MPa.

percentage of pillars was calculated using measured tap densities of carbon (0.21) and X7R powder (1.2). The dielectric constant of multilayer capacitors was decreased from 2400 to 1970 on increasing the pillar

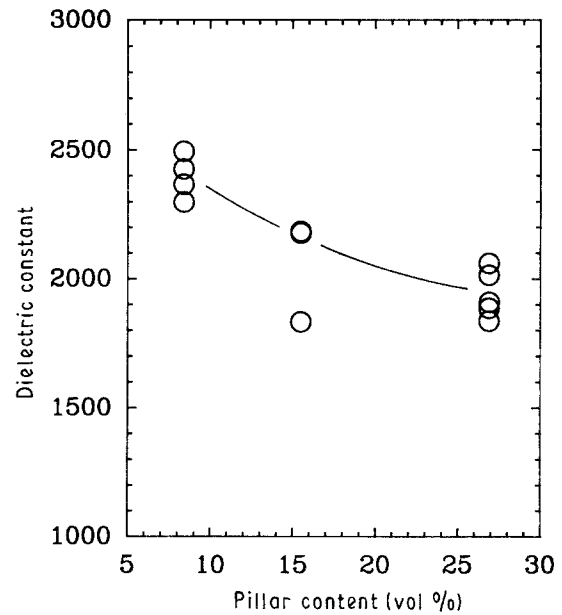


Figure 5 Dielectric constant of multilayer capacitors as a function of pillar content in the carbon paste to form the porous layers. For these samples, tin was infiltrated at 1.5 MPa for 1 min.

content from 8.4 vol % to 27 vol %. However, samples with lower pillar content were fragile and easily broken during handling. Thus, all the experiments to observe the infiltration behaviour were conducted with multilayer specimens containing 15.5 vol % pillars in the porous layers. As shown in a micrograph of a polished cross-section of multilayer sample (Fig. 6), porous layers were completely filled with tin electrode.

Fig. 7 shows the dielectric constant of chip samples with 15.5 vol % pillars in the porous layers at 40 °C, which were held in the tin melt bath of 260 °C for 1 min, as a function of infiltration pressure ranging from 0.2–1.5 MPa. Although tin infiltration into porous layers did not occur at all up to 0.35 MPa external pressure, complete infiltration to 10 mm long porous layers could be obtained with pressures above 0.5 MPa. For these samples, the external pressure was maintained below the melting point (232 °C) of tin during cooling after infiltration process. Thus, the

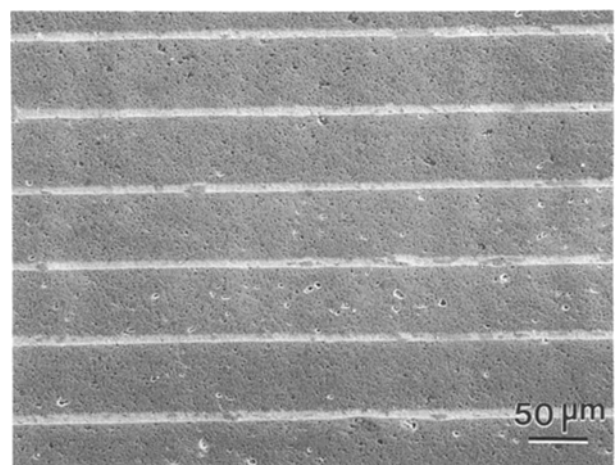


Figure 6 Scanning electron micrograph of a multilayer sample showing porous layers filled completely with tin by infiltration for 1 min at 1.5 MPa.

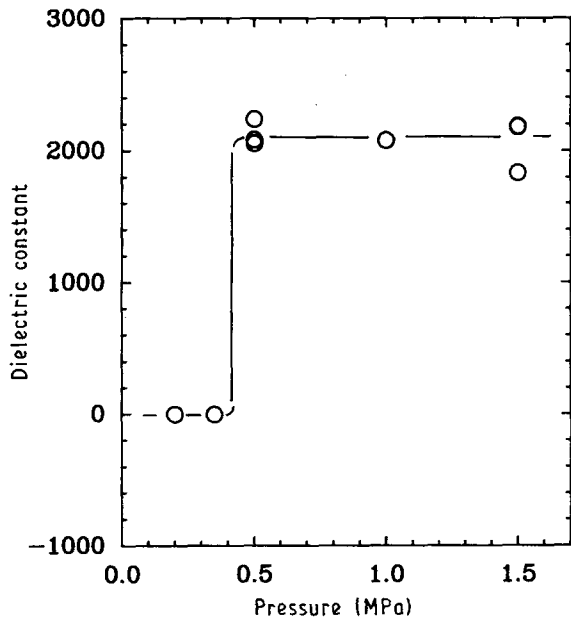


Figure 7 The variation of dielectric constant of multilayer capacitors, as a function of infiltration pressure, with tin infiltration for 1 min.

actual pressurized time for tin electrode in porous layers, which were infiltrated for 1 min in the tin melt bath, was about 20 min before solidification. After samples were withdrawn from the melt bath, the external pressure should be maintained to the temperature below the melting point of the electrode melt to prevent back-flow of the infiltrated melt from the porous layers due to the non-wetting characteristics of metals to ceramics. When the external pressure was removed immediately after samples were taken out of the tin melt bath after infiltration by dipping samples in the melt bath for 90 min at 1.5 MPa, tin melt was extruded out completely from the porous layers, leaving locally trapped tin between the ceramic pillars (Fig. 8).

To measure the accurate infiltration distance during dipping in the melt bath for 1 min by eliminating the movement of tin melt in the porous layers after withdrawing the samples from the melt bath, the external pressure was removed with the samples in the melt

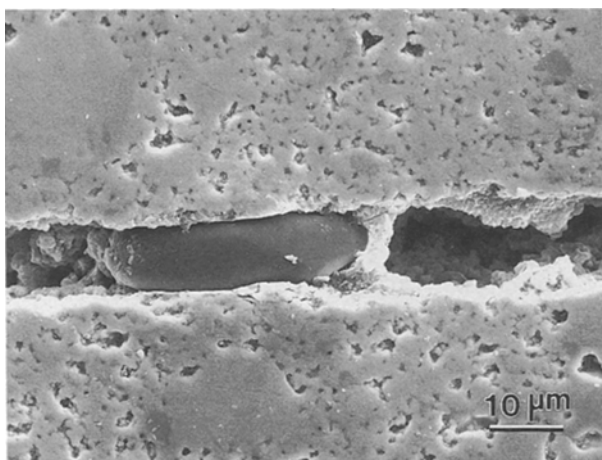


Figure 8 Scanning electron micrograph of a porous layer showing the complete back-flowing of the infiltrated tin melt out of the porous layer with a locally trapped tin electrode.

bath immediately after infiltration for 1 min. Then, the tin melt bath and samples were solidified and cut to observe the microstructure of the infiltrated samples. As infiltration to the porous layers cannot occur without an external pressure (Fig. 7) and the vacuum is maintained in the portion of the porous layers which is not filled with tin, the distance infiltrated with an external pressure is not changed by removing the external pressure while samples are in the melt bath. Using this method, it was confirmed that 10 mm long porous layers were completely infiltrated with tin at an external pressure higher than 0.5 MPa. This critical infiltration pressure may be varied by changing the electrode metal and the volume percentage of pillars in the porous layers.

With liquid infiltration into the porous solids [24–27], the infiltration behaviour of an electrode melt to the porous layers can be characterized by assuming that a porous layer, where pillars are randomly distributed, is formed by many cylindrical capillaries, as shown in Fig. 9. Considering the free-energy change of the total system (Equation 1), the critical infiltration pressure, P_{cr} , can be expressed as Equation 2 using Young's relation [26]

$$dF = -P_1 dV_1 - P_v dV_v + \gamma_{sl} dA_{sl} + \gamma_{sv} dA_{sv} < 0 \quad (1)$$

$$P_{cr} = -2\gamma_{lv} \cos\theta/r \quad (2)$$

where P_1 and P_v are the applied external pressure and the degree of the vacuum before infiltration, V_1 and V_v are the volume of the capillary occupied by the melt and vacuum, and A_{sl} and A_{sv} are the area contacted with the melt and vacuum, respectively. The surface tensions of the melt–vacuum, melt–ceramic, and ceramic–vacuum are γ_{lv} , γ_{sl} and γ_{sv} , respectively, θ is the wetting angle of the melt to the ceramic dielectrics, and r is the radius of the cylindrical capillaries formed by pillars in the porous layer. As tin shows complete non-wetting to BaTiO_3 ceramics and the surface tension of tin, γ_{lv} , at 332°C , is 543.8 mN m^{-1} [14], the smallest pore size formed by randomly distributed pillars in the porous layer can be estimated to be $4 \mu\text{m}$ with the critical infiltration pressure, P_{cr} , of 0.5 MPa (Fig. 7). This result is reasonable compared to the microstructure of pillars in a porous layer (Fig. 10).

The infiltration distance, x , for infiltration time, t , with external pressure, P_1 , can be expressed as [25, 26]

$$x = \left[\frac{r^2 t}{4\eta} (P_1 - P_{cr}) \right]^{1/2} \quad (3)$$

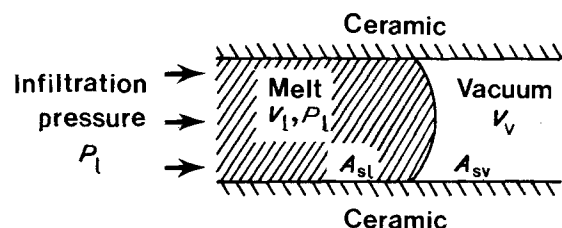


Figure 9 Schematic illustration of a cylindrical capillary into which molten electrode has infiltrated.

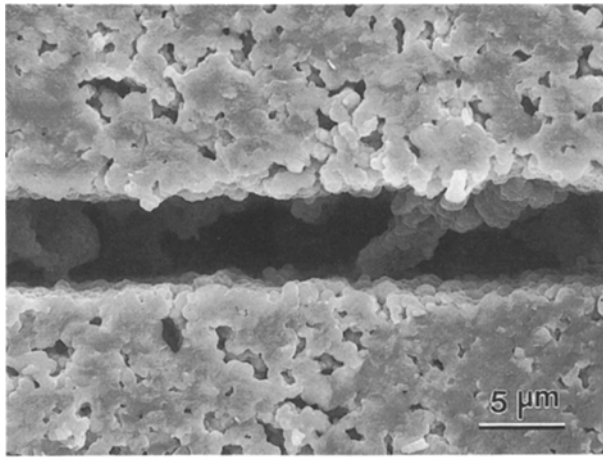


Figure 10 Scanning electron micrograph of a sintered chip showing the ceramic pillars in a porous layer.

where η is the dynamic viscosity of the infiltrated electrode. As shown in Fig. 11, where the dielectric constant of samples infiltrated at various pressures is illustrated as a function of infiltration time, 10 mm long porous layers were completely filled with tin melt for an infiltration time longer than 30 s at an applied pressure of 1.5 MPa. For an external pressure of 0.35 MPa, however, only local and discontinuous infiltration was observed even for 90 min holding of samples in the melt bath, which illustrates that the pressure is the most critical factor for the infiltration of an electrode metal to the porous layers.

3.3. Insulation resistance

The resistivity of 10^8 – $10^9 \Omega \text{cm}$, which is much lower than the value of conventional multilayer capacitors (10^{11} – $10^{12} \Omega \text{cm}$) where metal electrode is screen printed on dielectric green sheets and co-fired, was obtained for samples infiltrated at 1.5 MPa for 90 min. Fig. 12 shows a micro-defect on the surface of a sintered dielectric layer. The size and depth of the micro-defect, which was formed by indentation of solid particles in the carbon paste into the dielectric green sheet during the lamination process, is a few micrometres (Fig. 12). With an applied pressure

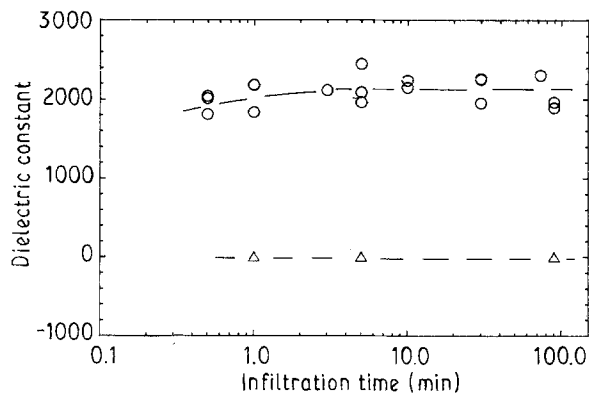


Figure 11 The variation of dielectric constant of electrode-infiltrated capacitors, as a function of infiltration time, at external pressures of (Δ) 0.35 and (\circ) 1.5 MPa.

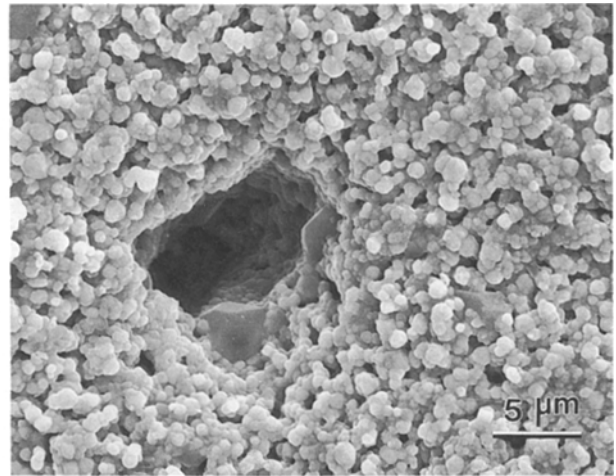


Figure 12 Scanning electron micrograph of a sintered dielectric layer showing a surface defect formed by indentation of a solid particle in the carbon paste into the dielectric green sheet during the lamination process.

during infiltration, however, this surface defect grew into the dielectric layer by stress concentration at the crack tip and was filled with the electrode melt (Fig. 13). The penetration of tin melt to a dielectric layer was often accelerated by the coalescence of the growing cracks with micro-pores in the dielectric ceramics. This lowered the insulation resistance and sometimes caused short samples. By controlling the infiltration pressure and time, insulation resistance could be improved. However, carbon particles and ceramic pillars in the carbon paste should be ground well, to prevent the formation of micro-defects on the surface of a dielectric green sheet during lamination. In addition, a denser microstructure of dielectrics than those used for conventional capacitors is required to improve the insulation resistance of multilayer capacitors by electrode infiltration.

4. Conclusions

1. With increasing adhesion of carbon paste to a dielectric green sheet stacked above it, a uniform

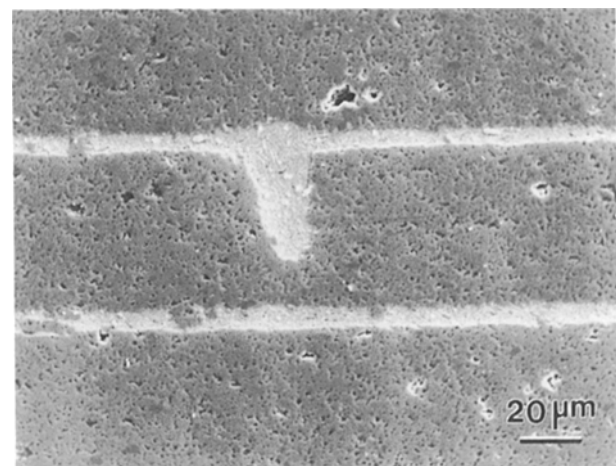


Figure 13 Scanning electron micrograph of a cross-sectioned multilayer capacitor showing the penetration of the tin electrode into the dielectric layer.

porous layers of 5 μm thickness was formed by preventing the green-state delamination between screen-printed carbon patterns and green tapes before sintering.

2. Compared to the dielectric constant of 2670 obtained for the disc-type sample, the dielectric constant of multilayer capacitors was lowered from 2400 to 1970 with the reduction of the actual electrode area by increasing the ceramic pillar content in the carbon paste for porous layers from 8.4 vol % to 27 vol %.

3. The external pressure was the most important parameter to determine the infiltration behaviour and the critical infiltration pressure of tin to the porous layers was found to be 0.5 MPa. The 5 μm thick porous layer, which was produced with the carbon paste where 15.5 vol % X7R particles were added as pillar materials, could be thought of as a porous solid formed by many pores larger than 4 μm .

4. The crack growth of micro-defects, which existed on the surface of a dielectric layer, by an external infiltration pressure, decreased the resistivity of multilayer samples to 10^8 – 10^9 Ωcm and sometimes caused short samples. To prevent the formation of micro-defects on the surface of ceramic green sheet by indentation of large particles in the carbon paste during the lamination process, solid particles, such as carbon and ceramic pillars, should be well ground during preparation of the carbon paste. In addition, slurry preparation and a sintering process to yield a denser dielectric microstructure than that used for conventional capacitors are required to improve the insulation resistance of multilayer capacitors by electrode infiltration.

References

1. R. C. BUCHANAN, in "Ceramic Materials for Electronics" (Marcel Dekker, New York, 1986) p. 98.
2. R. J. K. WASSINK, in "Soldering in Electronics" (Electrochemical Publications, Ayr, 1989) p. 390.
3. Y. SAKABE, *Amer. Ceram. Soc. Bull.* **66** (1987) 1338.
4. I. BURN and G. H. MAHER, *J. Mater. Sci.* **10** (1975) 633.
5. I. BURN, *Amer. Ceram. Soc. Bull.* **57** (1978) 600.
6. T. C. RUTT, US Pat. 3679 950 (1972).
7. *Idem.*, US Pat. 3829 356 (1974).
8. *Idem.*, US Pat. 4030 004 (1977).
9. R. GARCIA and R. H. MARION, US Pat. 4584 629 (1986).
10. Y. SAKABE, S. KARAKI and K. NAKANO, US Pat. 4652 967 (1987).
11. T. C. RUTT and J. A. STYNES, *IEEE Trans. Parts Hybrids and Packaging PHP-9* (1973) 144.
12. H. TAKAMIZAWA, K. UTSUMI, M. YONEZAWA and T. OHNO, *IEEE Trans. Comp. Hybrids and Manufact. Technol. CHMT-4* (1983) 355.
13. J. G. PEPIN, W. BARLAND, P'OCALLAGHAM and R. J. S. YOUNG, *J. Amer. Ceram. Soc.* **72** (1989) 2287.
14. J. Y. KOH, PhD thesis, Seoul National University, Korea (1989).
15. F. GOODENOUGH, *Electron. Design* **30** (1982) 35.
16. N. G. EROR, I. BURN and G. H. MAHER, US Pat. 3920 781 (1975).
17. J. H. ALEXANDER, UK Pat. GB 2103 422A (1981).
18. J. A. STYNES, US Pat. 4071 878 (1978).
19. T. C. RUTT and J. A. STYNES, US Pat. 3879 645 (1975).
20. T. C. RUTT, US Pat. 3965 552 (1976).
21. J. M. HERBERT, in "Ceramic Dielectrics and Capacitors" (Gordon and Breach Science, New York, 1985) p. 229.
22. M. YONEZAWA, *Amer. Ceram. Soc. Bull.* **62** (1983) 1375.
23. B. V. HIREMATH, R. E. NEWNHAM, L. E. CROSS and J. V. BIGGERS, *Adv. Ceram. Mater.* **3** (1988) 217.
24. V. BELTRAN, A. ESCARDINO, C. FELIU and MA D. RODRIGO, *Brit. Ceram. Trans. J.* **87** (1988) 64.
25. K. A. SEMLAK and F. N. RHINES, *AIME Trans.* **212** (1958) 325.
26. F. DELANNY, L. FROYEN and A. DERUYTTERE, *J. Mater. Sci.* **22** (1987) 1.
27. C. TOY and W. D. SCOTT, *J. Amer. Ceram. Soc.* **73** (1990) 97.

Received 9 July 1991

and accepted 17 February 1992